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Total Number of Pages in This Submission

Application Number	09/050,808
Filing Date	March 30, 1998
First Named Inventor	Yutaka Machida
Art Unit	2621
Examiner Name	Allen C. Wong
Attorney Docket No.	MAT-5860

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/Declaration(s)
- [x] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
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Date	December 4, 2006	*Registration No.*	34,515

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Signature	Deborah Spratt		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	09/050,808
Appellant:	Yutaka Machida
Filed:	March 30, 1998
Title:	DECODING AND CODING METHOD OF MOVING IMAGE SIGNAL, AND DECODING AND CODING APPARATUS OF MOVING IMAGE SIGNAL USING THE SAME
TC/A.U.:	2613
Examiner:	Allen C. Wong
Confirmation No.:	7277
Docket No.:	MAT-5860

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Further to the Request For Reinstatement of Appeal dated September 28, 2006, Appellant is submitting this Appeal Brief for the above-identified application.

I. REAL PARTY IN INTEREST

The real party in interest is Matsushita Electric Industrial Co., Ltd.

II. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

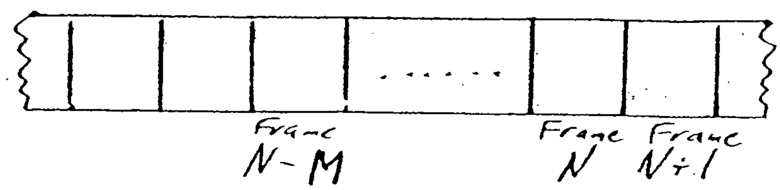
Claims 2, 7 and 12-22 are pending. Claims 1, 3-6 and 8-11 have been cancelled. Claims 2, 7 and 12-22 have been appealed.

IV. STATUS OF AMENDMENTS

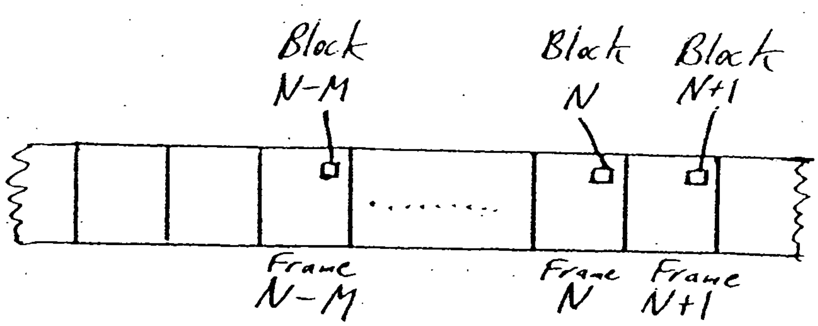
An Amendment after final rejection was filed on February 27, 2004. Appellant's representative argued that this Amendment did not raise new issues. The Examiner disagreed. Accordingly, that Amendment has not been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a method for decoding a block in a frame. The frame is one of a plurality of successive frames (Appellant's Fig. 2) in a predictively coded image signal. Thus, the plurality of frames may be referred to as frames N-M, N, and N+1 where M is ≧ 1. This is illustrated below.



The first step is to evaluate block N of frame N and block N-M of frame N-M (Appellant's specification, page 11, lines 23-26). Block N and block N-M are in corresponding locations. This is illustrated below:



An error is identified in block N or block N-M (Appellant's specification, page 12, lines 13-15).

If the error is identified in block N, then block N-M is used to decode block N+1. If the error is found in block N-M, then block N is used to decode block N+1 (Appellant's specification, page 13, lines 17-21).

An apparatus is also disclosed (and illustrated in Appellant's Fig 1) for performing the method set forth above. Thus, a detector evaluates block N (of frame N) and block N-M (of frame N-M). If the detector identifies an error in block N, then block N-M is used to decode block N+1. If the detector identifies an error in block N-M, then block N is used to decode block N+1.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 21 and 22 have been rejected under 35 U.S.C. §112, first paragraph. Claims 21 and 22 have been rejected under 35 U.S.C. §112, second paragraph. Claims 21 and 22 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Igarashi (U.S. 5,539,466) in view of Yamaguchi.

VIII. ARGUMENT

Claims 21 and 22 have been rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. In particular, the rejection argues that because Appellant's specification does not mention "specific terms" which are included in claims 21 and 22, that the claims fail to comply with the enablement requirements. This rejection is respectfully traversed. 35 U.S.C. §112, first paragraph does not require that a specification use the "specific terms" which are set forth in the claims. Furthermore, there is case law on point:

> The enablement requirement does not require that the patent disclose the specific embodiment of the claim; a broad claim can be enabled by the disclosure of a single embodiment.

Phillips Petroleum Co. v. U.S. Steel Corp., 673 F.Supp. 1278, aff'd. 865 F.2d 1247 (Fed.Cir. 1989).

Note that the Official Action was able to correctly summarize Appellant's claim. Furthermore, the Examiner has been able to perform an examination in both the most recent Official Action and in two Official Actions prior to the most recent

Official Action. In fact, claims 21 and 22 solidly meet the enablement requirement, so much that, Appellant's previous arguments were persuasive enough that previous appeals have been withdrawn. Accordingly, as there is no statutory requirement for a specification to mention "specific terms" set forth in claims, and, as Appellant's claims have been examined without the PTO raising any concern (several times), Appellant's claims 21 and 22 are patentable in view of 35 U.S.C. §112, first paragraph.

Claims 21 and 22 have been rejected under 35 U.S.C. §112, second paragraph. The rejection is respectfully traversed.

The rejection argues that if N=1 and M=1, then the claim would read on a "frame 0." The rejection further argues that "frame 0" is a non-existent frame. The rejection concludes that since "frame 0" is a non-existent frame, claim 21 is therefore "omitting essential elements." The rejection is respectfully traversed.

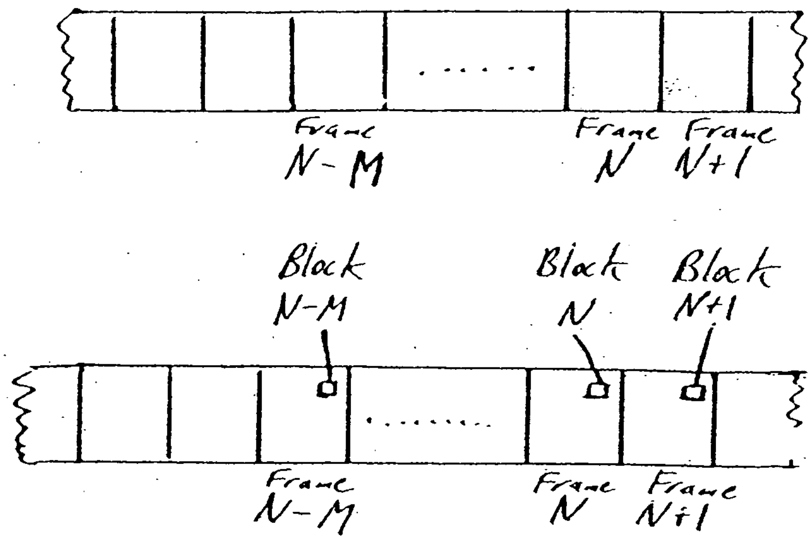
Identifying a frame as frame 0 does not make the frame "non-existent." The frame number is merely an index for identifying the frame relative to other frames. Furthermore, identifying a frame as "frame 0" is well known in the art. In the Evidence Appendix, Appellant includes a portion of the technical specifications for the Sega video game of the 1980's. The specification identifies various different frames including, for example, "frame 0." Accordingly, the rejection is wrong by describing "frame 0" as being a non-existent frame. Reversal of the rejection is respectfully requested.

Claims 21 and 22 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Igarashi (U.S. 5,539,466) in view of Yamaguchi.

Appellant's invention, as recited by claim 21, includes a feature which is neither disclosed nor suggested by the art of record, namely:

> ... evaluating block N ... wherein blocks N-M, N and N+1 are in corresponding locations of frames N-M, N and N+1, respectively.

As set forth in the previous two Appeal Briefs, this is illustrated as shown below.



For a reference to be properly used to reject Appellant's claim 21, the reference would need to show a block in three corresponding locations of three respective frames (which is what is shown in the Brief above). The Examiner argues that blocks in corresponding locations of frames is disclosed by Igarashi. In particular, the Examiner refers to Fig. 6 of Igarashi. Fig. 6 of Igarashi illustrates a block occupying a corresponding location in <u>two</u> frames. Appellant, however, by claiming corresponding locations in frame N-M, frame N and frame N+1, claims blocks in corresponding locations of <u>three</u> frames. As Igarashi only discloses a block in corresponding locations of two frames (and not Appellant's claimed blocks in corresponding location of three frames), Igarashi is not a proper reference to reject Appellant's claims.

The Examiner rejects Appellant's claims by combining Igarashi with Yamaguchi. Appellant respectfully disagrees with the citation of Yamaguchi against Appellant's claims. The Official Action argues that col. 8, line 30 of Yamaguchi discloses front prediction and rear prediction. Front prediction and rear prediction, however, have nothing to do with Appellant's claimed error correction. The Official Action refers to error correction in Yamaguchi, col. 8, lines 15-28. Appellant's error correction is claimed as occurring in <u>different frames</u>. The error correction at lines 15-28 of Yamaguchi, however, does not occur in <u>different frames</u>. Rather, the error

correction illustrated by Yamaguchi, Fig. 8A shows that a error in a block X is corrected by an adjacent block (see col. 8, line 23). Correcting an error based on the contents of an adjacent block has nothing to do with Appellant's claimed feature of correcting an error based on blocks in previous frames. Accordingly, claim 21 is patentable over the combination of Igarashi and Yamaguchi.

Claim 22 is patentable by virtue of its dependency on claim 21.

In view of the arguments set forth above, allowance of claims 21 and 22 is respectfully requested.

Respectfully Submitted,

RatnerPrestia

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LEA/ds

Enclosures: Pending claims
Evidence Appendix
Reiated Proceedings Index

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The Assistant Commissioner is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

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Deborah Spratt

ds/89770

APPENDIX OF CLAIMS

1. (Cancelled)

2. (Previously Presented) The method of decoding an image signal of claim 12, wherein if the predicted pixel blocks are free from decoding error,

the predicted pixel blocks produced from a latest decoded frame is used in reconstruction of the present pixel block.

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Previously Presented) The decoding apparatus of claim 20, wherein the means for storing stores bit errors of plural video frames by plotting pixel blocks in which bit error is detected in each video frame in a form of decoding error maps.

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Previously Presented) A method of decoding block N+1 according to claim 21, wherein the image signal is a bit stream of a coded compressed video signal, the method further comprising the steps of:

decoding the bit stream for information defining pixel blocks, the information including motion vectors;

step b) includes the step of detecting an error in the information of one of the pixel blocks being blocks N and N-M in each of at least two frames which are prior to a present frame said present frame being frame N+1, said at least two frames being frames N and N-M;

storing error information of the one of the pixel blocks in each of the at least two frames which are prior to the present frame, in an error memory;

storing, in a frame memory, video information of the at least two frames which are prior to a present frame;

generating from the decoded motion vectors at least two predicted pixel blocks corresponding to a present pixel block in the present frame;

step b) further includes the step of judging if one of the at least two predicted pixel blocks corresponds to error information of the at least two frames stored in the error memory; and

step c) includes the step of using one of the at least two predicted pixel blocks in reconstructing the present pixel block based on the judging.

13. (Previously Presented) The method for decoding an image signal of claim 12, wherein each of the predicted pixel blocks is generated from reconstructed video frames by using motion vectors which correspond to the reconstructed video frames.

14. (Previously Presented) The method for decoding an image signal of claim 12, wherein if one of the at least two predicted pixel blocks is judged to correspond to error information stored in the error memory, the other of the at least two predicted pixel blocks is used in reconstruction of the present pixel block.

15. (Previously Presented) The method of decoding an image signal of claim 12, wherein if the at least two predicted pixel blocks are judged not to correspond to error information stored in the error memory, an average of the at least two predicted pixel blocks is used in reconstructing of the present pixel block.

16. (Previously Presented) A method of decoding block N+1 according to claim 21, said method further for reconstructing video frames of the image signal, the method further comprising the steps of:

decoding the image signal for information to define pixel blocks of video frames, the information including motion vectors;

step b) includes the step of generating decoding error maps indicating decoding errors of pixel blocks being blocks N and N-M in each of at least two

frames which are prior to a present video frame said present frame being frame N+1, said at least two frames being frames N and N-M;

storing the decoding error maps in error memory;

storing, in a frame memory, video information of the at least two frames which are prior in time to the present video frame;

generating from the decoded motion vectors at least two predicted pixel blocks corresponding to a present pixel block in the present video frame; and

step b) further includes the steps of determining if a predicted pixel block includes decoding errors corresponding to decoding errors in either of the at least two frames which are prior to the present frame; and based on the determining, judging if the predicted pixel block is used in reconstructing the present video block.

17. (Previously Presented) A decoding apparatus according to claim 22, wherein said detector includes

a decoding device for decoding the image signal to define pixel blocks of video frames, the image signal including motion vectors;

means for detecting decoding errors of the pixel blocks being blocks N and N-M in each of at least two frames which are prior to a present video frame said present frame being frame N+1, said at least two frames being frames N and N-M;

an error memory for storing decoding error maps of the decoding errors of the pixel blocks in each of the at least two frames which are prior to the present frame;

motion compensation means for generating from the decoded motion vectors at least two predicted pixel blocks corresponding to a present block which is block N+1 in a present video frame which is frame N+1; and

predicted image selecting means, based on the decoding error maps, determining if the predicted pixel blocks include decoding errors corresponding to decoding errors in either of the at least two frames which are prior to the present frame, and thereby determining use of the predicted pixel blocks in reconstructing the present block.

18. (Previously Presented) The decoding apparatus of claim 17, wherein the video signal is a bit stream of variable length code, and the decoding device separates and decodes the variable length code from the bit stream and writes presence or absence of decoding errors in the decoding error maps.

19. (Previously Presented) The decoding apparatus of claim 17, wherein the motion compensation means generates one predicted pixel block based on a reconstructed video frame which is one frame before the present frame, and generates another predicted pixel block based on a reconstructed video frame which is two frames before the present frame.

20. (Previously Presented) A decoding apparatus according to claim 22, wherein said detector includes

means for decoding the bit stream for information defining pixel blocks, the information including motion vectors;

means for detecting an error in the information of one of the pixel blocks being blocks N and N-M in each of at least two frames which are prior to a present frame said present frame being frame N+1, said at least two frames being frames N and N-M;

means for storing error information of the one of the pixel blocks in each of the at least two frames which are prior to the present frame;

means for storing video information of the at least two frames which are prior to a present frame;

means for generating from the decoded motion vectors at least two predicted pixel blocks corresponding to a present pixel block which is block N+1 in the present frame;

means for judging if one of the at least two predicted pixel blocks corresponds to error information of the at least two frames stored in the means for storing; and

means for determining if the one of the at least two predicted pixel blocks is used in reconstructing the present block, based on judging of the means for judging.

21. (Previously Presented) A method of decoding block N+1 in frame N+1 of successive frames of a predictively coded image signal, said method comprising the steps of:

a) evaluating block N of frame N and block N-M of frame N-M of said signal, wherein blocks N-M, N and N+1 are in corresponding locations of frames N-M, N and N+1, respectively, M=>1;

b) identifying an error in one of block N and block N-M;

c) using the other of block N and block N-M to decode block N+1.

22. (Previously Presented) Apparatus for decoding block N+1 in frame N+1 of successive frames of a predictively coded image signal, said apparatus comprising:

a detector for evaluating block N of frame N and block N-M of frame N-M of said signal, wherein blocks N-M, N and N+1 are in corresponding locations of frames N-M, N and N+1, respectively, M=>1 and for identifying an error in one of block N and block N-M; and

a decoder for using the other of block N and block N-M to decode block N+1.

EVIDENCE APPENDIX

SMSARCH: A Sega Master System Cartridge Archiver

SMSARCH: A Sega Master System Cartridge Archiver

1.0 Introduction

The SMSARCH is a Sega Master System cartridge archiver. The device copies the contents of the cartridge ROM to a binary file by interfacing with a personal computer. The interface is through a 25-pin Centronics parallel port. One major design goal was to have the device's hardware be as simple as possible. Therefore, most of the SMSARCH's control is implemented in software. The software uses the parallel port's control lines to communicate with the SMSARCH's hardware. Also, the software makes special use of the parallel port's printer status lines, allowing the SMSARCH to be used with any parallel port (a bi-directional port is not necessary). The software is written in C++.

2.0 Sega Master System Technical Overview

The Sega Master System (SMS) is an 8-bit video-game console that was introduced in the U.S. in 1986. The console uses a Z80 microprocessor as its main processor. The SMS has 8 kilobytes of program RAM and 16 kilobytes of video RAM. Additionally, the SMS can handle ROM's up to 4 Megabits (512 kilobytes). Only the program RAM and cartridge ROM areas are directly addressed by the Z80 microprocessor. The video RAM is addressed through hardware ports. Accessing a cartridge's entire ROM area requires special paging due to the Z80's limited 16-bit address size. The SMSARCH emulates the functions of the SMS's paging hardware allowing it to access all of a cartridge's ROM contents.

2.1 The Sega Master System's Paging Scheme

The SMS's main processor, the Z80, can address up to 64 kilobytes of memory (the Z80 supports 16-bit addresses). Some of the memory is mapped to RAM, and some is mapped to ROM. This ROM is the game ROM. Sega Master System ROM's comes in two forms. The first are ROM cards, (or "Sega Cards"), that are physically about the size of credit cards. These compact ROM's can hold 32 kilobytes of data. The most popular ROM format for the SMS, however, is cartridges. Cartridges come in 1, 2, and 4 megabit (128, 256, and 512 kilobyte) sizes. Because the ROM cartridges can be much larger than 64 kilobytes, the SMS makes use of a special paging scheme that maps 16-kilobyte pages into 16-kilobyte frames in main memory. The main memory map is shown in figure 1.

The SMS uses three 16-kilobyte frames, allowing a total of 48 kilobytes of ROM to be "visible" at a time. Therefore, although an entire ROM card's memory is visible at any time, only a fraction of the total ROM on a cartridge is visible. To access the entire contents of a ROM cartridge it is necessary to swap pages in and out of the frames, as they are needed. This is accomplished through three "Frame Control Registers," or FCR's. The FCR's are located at addresses 0xFFFD, 0xFFFE, 0xFFFF hexadecimal. Writing the desired page number to these registers will cause that page to appear in the respective frame. Note, that in practice, the largest number ever written to these registers is 31 (addressing starts at 0), because the largest cartridge ever manufactured was 4 megabits (512 kilobytes, or 32 16-kilobyte pages). However, because they are 8-bit registers, it is very likely that the SMS could support cartridges with as many as 256 pages. This would yield cartridges with sizes up to 32 megabits (4 megabytes). Another point is that the FCR's are physically located on the cartridge. This can lead to differences in the way the actual paging mechanism works, depending on the cartridge. As we will see later, this is exactly the case. The general paging scheme mentioned in this paragraph is made slightly more complicated depending on the size of a cartridge, as discussed in the section titled 'How Cartridges Handle Paging.'

Starting Address (hexadecimal)	Description
0x0000	First 1 kilobyte of ROM page 0
0x0400	Frame 0, (Last 15 kilobytes, first kilobyte is always from page 0)
0x4000	Frame 1
0x8000	Frame 2
0xC000	Program RAM
0xE000	Mirror of Program RAM (minus last four bytes)
0xFFFC	Control byte for Frame 2 (described below)
0xFFFD	Page to go into Frame 0. (Only last 15 kilobytes of selected page. The first kilobyte is always from ROM page 0.)
0xFFFE	Page to go into Frame 1
0xFFFF	Page to go into Frame 2

Figure 1: Sega Master System Main Memory Map

There are other complications as well. Notice that Frame 0 is really only a 15-kilobyte frame. When the system is powered on, the values of the FCR's can not be controlled. Therefore, a known area of ROM must be provided so the system can initialize itself. By forcing the first 1-kilobyte of memory to always point to ROM page 0, the system always knows where its start-up code is, regardless of the contents of the FCR's. Consequently, any initialization and start-up code must be placed in the first 1 kilobyte of ROM page 0. Although this is an effective way of guaranteeing proper power up, it limits the usefulness of frame 0. Only the last 15 kilobytes of any page mapped into frame 0 will be available. The first kilobyte will always be from ROM page 0.

The SMS has the capability of including "Battery-backed-up RAM" on a cartridge. This allows the user to save the current game on the cartridge, and continue even after the console's power has been turned off. Accessing this RAM is accomplished using Frame 2. The FCR 0xFFFC controls whether Frame 2 will contain a page of ROM or a page of battery-backed-up RAM. Only Frame 2 has this feature. The bit fields for 0xFFFC are shown in figure 2.

Bit Field	Function
7-4	Unknown
3	16K RAM or ROM (0=ROM, 1=RAM)
2	RAM page 0 or 1
1-0	Unknown

RELATED PROCEEDINGS INDEX

None